

WHAT IS CLAIMED IS:

1. An LOC type semiconductor package, comprising:  
a semiconductor chip on which a plurality of bonding pads are arranged in a row;  
leads that correspond to the bonding pads, the leads being located on opposite sides of  
the semiconductor chip with the bonding pads therebetween;  
wires electrically connecting the bonding pads to the leads; and  
a molding resin encapsulating the semiconductor chip, leads and wires, wherein:  
the leads include general leads and a pair of stable leads;  
the stable leads are electrically connected to the bonding pads via the wires, disposed  
at opposite ends of the semiconductor chip, and bent to extend toward the semiconductor chip  
and physically contact the semiconductor chip to fix the semiconductor chip; and  
the general leads are disposed in a row between the stable leads, electrically  
connected to the bonding pads by way of the wires, and separated from the semiconductor  
chip, coming into no contact with the semiconductor chip.
2. The LOC type semiconductor package as claimed in claim 1, wherein:  
the general leads include general inner leads encapsulated in the molding resin and  
general outer leads extending from the molding; and  
the stable leads include stable inner leads encapsulated in the molding resin and stable  
outer leads extending from the molding resin.
3. The LOC type semiconductor package as claimed in claim 2, wherein an adhesive  
member is on the portion of the surface of the semiconductor chip, corresponding to the end  
of each of the stable inner leads, to fix the end of the stable inner lead onto the surface of the  
semiconductor chip.
4. The LOC type semiconductor package as claimed in claim 3, wherein the surface  
area of the end of the stable inner lead coming into contact with the adhesive member is  
substantially wider than a portion of the stable inner lead that does not contact the adhesive  
member.
5. The LOC type semiconductor package as claimed in claim 2, wherein the ends of  
the general inner leads are up-set toward the top of the semiconductor chip.

6. A manufacturing process comprising:  
producing a plurality of lead frames for chip packages, each of the lead frames having the same structure;

5 mounting a first semiconductor chip on a first of the lead frames for packaging of the first semiconductor chip, the first semiconductor chip having a first size; and

mounting a second semiconductor chip on a second of the lead frames for packaging of the second semiconductor chip, the second semiconductor chip having a second size that differs from the first size.

10 7. The process of claim 6, wherein:

each of the lead frames comprises stable leads and general leads;

5 mounting the first semiconductor chip comprises attaching the stable leads of the first lead frame to a surface of the first semiconductor chip while the general leads of the first lead frame remain separated from the first semiconductor chip; and

mounting the second semiconductor chip comprises attaching the stable leads of the second lead frame to a surface of the second semiconductor chip while the general leads of the second lead frame remain separated from the second semiconductor chip.

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